AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A self-synchronous transfer control circuit, comprising:

a transfer control circuit transferring a first pulse applied from a preceding stage to a subsequent stage as a second pulse based on an instruction signal instructing enabling or disabling a transfer; and

a pulse control circuit receiving one data transfer request pulse signal as said first pulse from said transfer control circuit in the preceding stage to output a plurality of data transfer request pulse signals as said second pulse to the transfer control circuit in the subsequent stage,

wherein the transfer control circuit, the transfer control circuit in the preceding stage, and the transfer control circuit in the subsequent stage are substantially, similarly configured.

2. (Original) The self-synchronous transfer control circuit according to claim 1, further comprising:

a data number setting means setting the number of data transferred to said transfer control circuit in the subsequent stage.

3. (Original) The self-synchronous transfer control circuit according to claim 2, wherein said pulse control circuit includes

a first logic circuit outputting a transfer enabling pulse signal to said transfer control circuit in the preceding stage as a third pulse, in response to application of said data transfer request pulse signal from said transfer control circuit in the preceding stage,

a second logic circuit outputting data transfer request pulse signal to said transfer control circuit in the subsequent stage,

a storage circuit storing the number of data in response to setting of the number of data by said data number setting means,

a gate circuit receiving a transfer enabling signal as a fourth pulse from said transfer control circuit in the subsequent stage and,

a transfer circuit outputting said transfer request pulse signal from said second logic circuit by the number of data stored in said storage circuit every time said gate circuit receives

said transfer enabling signal, in response to application of said data transfer request pulse signal to said first logic circuit, when said number of data is stored in said storage circuit.

4. (Original) The self-synchronous transfer control circuit according to clam 3, wherein said pulse control circuit includes

a counter circuit counting the number of times said transfer request pulse signal is output, and

a disabling circuit comparing the counter output of said counter circuit with the number of data stored in said storage circuit to disable the output of said transfer request pulse signal by said transfer circuit, in response to correspondence thereof.

5. (Previously Presented) A data driven information processing device, using a self-synchronous transfer control circuit receiving one data transfer request pulse signal indicating request of transfer from a transfer control circuit in a preceding stage to output a plurality of transfer request pulse signals to a transfer control circuit in a subsequent stage, comprising:

a data transmission path holding a data packet based on a pulse signal applied from said self-synchronous transfer control circuit; and

a data number detection means for detecting the number of data based on output packet information set to the data packet held in said data transmission path,

said self-synchronous transfer control circuit outputting a transfer request pulse signal corresponding to the number of data, in response to detection of the number of data by said data number detection means.

6. (Original) The data driven information processing device according to claim 5, wherein

said data transmission path holds a data packet including a destination field storing at least destination information, an instruction field storing instruction information and a data field storing data; and

said data number detection means transmits, in response to detection that a copying instruction is present in an instruction field included in the data packet held in said data transmission path, data copied from the data transmission path in a subsequent stage.

7. (Original) The data driven information processing device according to claim 6, wherein

a data number detection means transmits a plurality of data packets having the same data as the data in a data field included in the data packet and having destination information different from each other, from the data transmission path to the data transmission path in a subsequent stage, in response to detection of said copying instruction.

8. (Original) The data driven information processing device according to claim 6, wherein

said data number detection means transmits a plurality of data packets different from data packet from the data transmission path to a data transmission path in a subsequent stage, in response to detection of said copying instruction.

9. (Previously Presented) The data driven information processing device of claim 5, wherein the pulse signal is not a clock signal.

10. (Previously Presented) The data driven information processing device of claim 1, wherein the output of the plurality of data transfer request pulse signals is a copying process.

11. (New) The self-synchronous transfer control circuit as set forth in claim 1, wherein the transfer control circuit transferring a first pulse applied from a preceding stage to a subsequent stage as a second pulse is self-synchronous.